Effect of local grain distribution and Enhancement on edgebond applied wafer-level chip-scale package (WLCSP) thermal cycling performance

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Abstract— **The demand on reliable Wafer level chip scale packages (WLCSP) are getting higher due to the need of small form factor and cost. As demonstrated in earlier publications the degradation and deformation mechanism show microstructure evolution associated with the thermal cycling induced damage accumulation. The mechanism, leading to crack initiation and propagation during thermal cycling by sub-grain boundary development can be observed as a general damage accumulation mechanism in various solder joints. The correlation between crack propagation and localized recrystallization are compared in a series of cross section analyses on thermal cycled WLCSP components with normal and elevated temperature thermal cycling conditions. Damage accumulated solder joint locations are identified and an attempt of using edge-bond materials to strengthen the localized solder joints demonstrate that the T_g and CTE needs adjustment to have the thermal cycling performance enhancement. Edge-bond material applied components show either a shift of damage accumulation to a more localized region, thus potentially accelerated the degradation, or mitigate the distribution resulting in an enhancement of thermal cycling based on their T_g and CTE properties. The edge-bond applied WLCSPs were thermally cycled from 0^oC to 100^oC with 10min. dwell time, and to simulate the function temperature environment, components were also tested at elevated temperature cycles for comparison. Using an analysis on localized distribution of recrystallized areas inside the solder joint provide more information on the localized microstructure evolution during thermal cycling. The results show that the crack propagation distribution and recrystallization region correlation can explain the enhancement and potential degradation mechanisms and support the damage accumulation history in a more efficient way.**

Keywords- WLCSP, Grain microstructure, Edge-bond, Thermal cycling

I. INTRODUCTION

Electronic packages show their own thermal cycling performance based on various factors, like die size, substrate material, solder joint alloy, surface finish and ball pitch etc. A general distribution of various package type depended lifecycles on a few different board thicknesses is shown in Figure 1, where the thermal cycling condition was the same for all packages, which were tested with a 0^oC to 100^oC thermal cycling profile with a 10min dwell time. As shown in the figure, in general, WLCSPs or CSP packages show relatively shorter characteristic lifecycle numbers subject to thermal cycling, since the higher CTE mismatch. The mechanism, leading to crack initiation and propagation during thermal cycling by sub-grain boundary development can be observed as a general damage accumulation mechanism. [1,2] In earlier publications the degradation and deformation mechanism were studied and showed the microstructure evolution associated with the thermal cycling induced damage accumulation.[2] Figure 2 illustrates the development of an microstructure evolution in thermally cycled WLCSP, analyzed with Orientation image microscopy (OIM) compared to crack propagation rate and recrystallization areas.[1] A wide distribution of recrystallized grains after thermally cycled WLCSP can be seen in most of the solder joints. The associated crack propagation is also observed in most of the joints. Using this methodology observing the grain structure evolution during
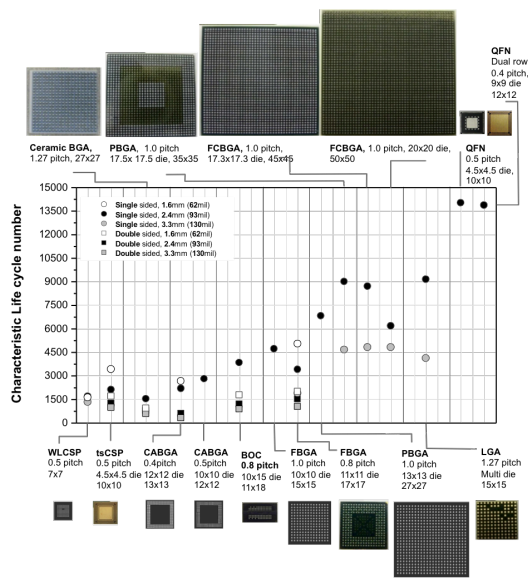
Figure 1. Characteristic thermal cycling life cycle number depends on the package design. Solder alloy for all packages are SAC305.[1]
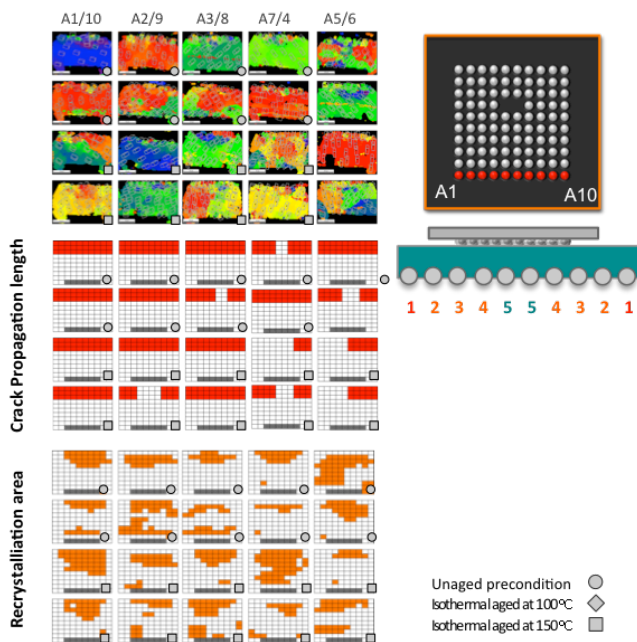

Figure 2. Selected WLCSP joints examined after thermal cycling to failure close the characteristic cycle number with OIM and corresponding characterization of observed crack length (indicated by red bars on corresponding grids) and locations of recrystallized grains (indicated by orange cells on corresponding grids) [1]

or after thermal cycling can indicate the stressed/strained damage solder joints and give a more detailed information whether the joints are under a high risk location or not. The rate that this process occurs depends on the package design and configuration, but using the crack propagation path and regions, which are recrystallized during thermal cycling can explain additional phenomenon and mechanism associated with the certain package configuration and associated thermal cycling process. [1-3] As seen in the example with WLCSP most of the solder joints indicated a vast accumulation of strain and recrystallization induced by thermal cycling, resulting in a relatively short characteristic life.[1,3] But at the same time, the demand of the WLCSP is getting higher due to the need of small form factor and cost. Improving the thermal cycling performance of WLCSP can be achieved by roughly three categorized approaches, the first is the strengthening of the solder joint by applying a new solder alloy composition, which can perform well in thermal cycling. The second approach is the enhancement of the total package, which is the use of underfill material. Even if it is a mature technology, the underfill process at the BGA board level component has a few challenges associated with no-clean flux residue, which can negatively impact the interface between the underfill material and the board interface. The re-workability of large underfilled components is also a factor, which needs to be thoroughly considered. The third approach is a localized enhancement using edge-bond materials. The outer array solder joints experienced most of the damage accumulation during thermal cycling, thus an enhancement targeting those solder joints can result in a higher thermal cycling performance. WLCSPs were on the market for a long time but with the new application and increased complexity, a detailed look into the solder joint degradation mechanism was revisited with a simple application of edge-bond materials to enhance the thermal cycling performance. Monitoring and following the grain structure evolution, one might be able to assess the failure mechanism associated with the critical solder joint location in the given package. With quantitative approach to identifying the grain structure evolution, the recrystallized area can be used as a damage accumulation indicator. The higher rate of Grain refinement and recrystallization indicated that, which solder joint is the most damaged during thermal cycling and able to give feedback, allow whether that the specific joint needs enhancement. Another factor considered in this paper and evaluation process is the function temperature of the device. Since WLCSP packages are directly exposed to air, the temperature of the package can directly impact the edge-bond materials attached to the device. Thus a test at an elevated temperature is fair to

include in the evaluation process. To achieve the elevated temperature environment, a heating layer was embedded in the PCB to increase the overall temperature to 50°C. The paper presented here is on localized solder enhancement using edge-bond materials to improve the thermal cycling performance at normal temperature and elevated temperature environment.
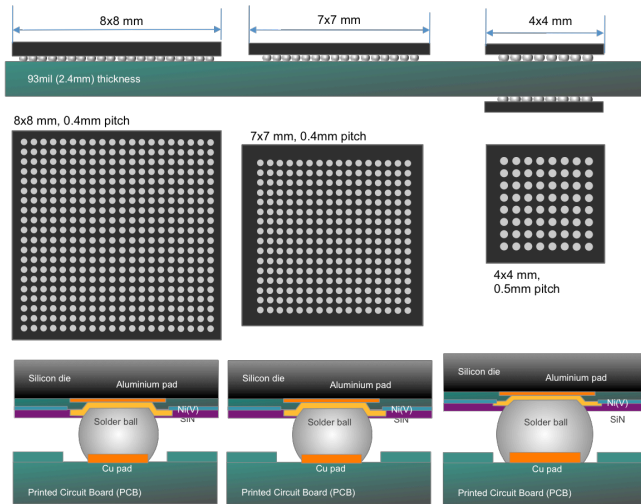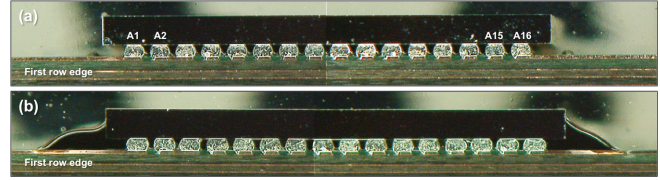

Figure 4. Cross section side view and Top after placing the edgebond (A) material. (a) no-material applied component (b) edgebond material applied component. [2]

Figure 3. WLCSP sample configuration and solder ball array schematics. Three types of WLCSP used in this study. 8x8mm, 7x7mm and 4x4mm.

II. EXPERIMENTAL PROCEDURE

Three WLCSP configurations were used in this study. 4x4mm, 7x7mm and 8x8mm WLCSP sample configuration with 0.5-mm pitch for 4x4 mm configuration and 0.4mm pitch for 7x7mm and 8x8mm WLCSPs. A schematic diagram of each sample configuration is shown in Figure 3. Solder balls attached to the packages were all composed of Sn-3.0Ag-0.5Cu (wt%) (SAC305). The parts were board-assembled on 93mil (2.4 mm) thick high glass transition temperature (T_g), FR4-printed circuit boards featuring Cu pads with organic surface preservative (OSP) surface finishes with typical peak temperatures of 240 °C, 60 seconds above the liquidus temperature reflow profile. All components were assembled with SAC305 solder paste. For edge-bond process, commercially available edge-bond adhesive were selected. Two types of edge-bond material were used in this study. The T_g and CTE were 30°C and 70ppm/°C respectively for the earlier experiment and

evaluation (indicated as edge-bond A), and a material to compare the thermal cycling performance, a higher T_g, 130°C and lower CTE, 30ppm/°C edge-bond material (edge-bond B), provided by Zymet, was used for the 8x8mm WLCSP samples. To prevent voiding due to moisture releasing from PCB material in curing cycle, test boards are pre-baked for 4 hours at 125°C. The edge-bond adhesives were dispensed at room temperature using a pneumatic, hand-held dispenser on each of the four corners. Each leg of adhesive was 1.8mm in length for the 7x7mm WLCSP and 2.0mm for the 8x8mm WLCSPs, which covered 25% of the WLCSP edge. The board was then cured at 150°C for 30 minutes. The cross-section side view pictures after placing the edge-bond for the 7x7mm WLCSP, is shown in Figure 4. The edge-bond material did not penetrated into the BGA array under the component, only forming a bonding between the bottom side edge and corner of the component to the PCB surface. For thermal cycling, samples were cycled from 0 to 100 °C at a ramp rate of 10 °C per minute with 10 minutes of dwell time. A continuous resistivity measurement using a data logger was applied for each channel in situ monitoring during the test. The failure criterion in this study was based on the JESD22-A104D standard [4], a 20% increase of the peak resistivity for continuous five cycles relative to the initial value. The results were plotted as Weibull distribution plots. Cross-sectional analysis using optical microscope with bright light and polarized light were applied to observe the evolution of the microstructures and the locations of the solder joint cracks.

III. RESULTS AND DISCUSSION

The characteristic lifecycle number for 8x8mm WLCSP was 638 cycles, with a first failure at 331 cycles. The characteristic cycle number for 7x7mm WLCSP and first failure was 792 cycles and 513 cycles respectively. On the other hand, the 4x4mm WLCSP with a double-sided assembly configuration show a characteristic life and first

failure cycle at 5650 and 3810 cycles respectively. It is shown that a smaller die size resulted in a longer life cycle number as expected, due to the fact that CTE mismatch is smaller in case of smaller die size. Since the 4x4mm WLCSP performs well under thermal cycling conditions, 7x7mm and 8x8mm samples were selected for edge-bond material application. The characteristic life cycle number for edge-bond A material applied 7x7mm samples was 387 cycles. The results were published in an earlier publication [2] and show actually a degraded performance of 38%. It was concluded that Edge-bond A material property with a low Tg and high CTE was not a good combination for the WLCSP thermal cycling performance. The edge-bond material applied to the edge of the WLCSP did protection to the first corner solder joint but induced accelerated damage accumulation at the second solder joint from the corner as shown in Figure 5. A fine grain structure development can be seen in no edge-bond applied WLCSP sample in Figure 5(a) at joint A1 and A2 where the crack propagated. This observation indicated that no edge-bond material applied solder joints experienced a normal strain induced damage accumulation at the corner joints, resulting in crack propagation at the package side interface. But compared to the Figure 6(a) and (c), the edge-bond A material applied joints did not show an extensive grain refinement at the corner joints and actually show a crack propagation at the board side interface. As shown in Figure 6(d), the upper portion of the solder joint A1 and A2 were protected and stabilized. This can be identified since there was no recrystallized grain structure development observed at the upper region of the solder joint (A1). It seems that during thermal cycling the main damage accumulation site was shifted to a localized area near the board side interface, resulting in a faster crack propagation rate and failure. This phenomenon shows that the use of lower T_g and higher CTE accelerated the failure progress rate and induced faster localized degradation. To improve the thermal cycling performance a higher Tg and lower CTE edge-bond is desired and need to be implemented. For that reason a higher Tg material with 130°C and a lower CTE material with 30ppm/^{o}C was introduced and used in the 8x8mm WLCSP test vehicle. Figure 6 shows the SEM picture of the initial microstructure of the 8x8mm WLCSP solder interconnect. The interface structure revealed an intermetallic compound (IMC) structure layer with 2μm at both package and board side interfaces. Even with the content of Ni the IMC shape were near scallop type for both sides. To achieve an elevated temperature environment additional to the thermal cycling temperature, a heating element at the fourth layer of the PCB was implemented in an eight layer PCB. The heater was able to bring up the
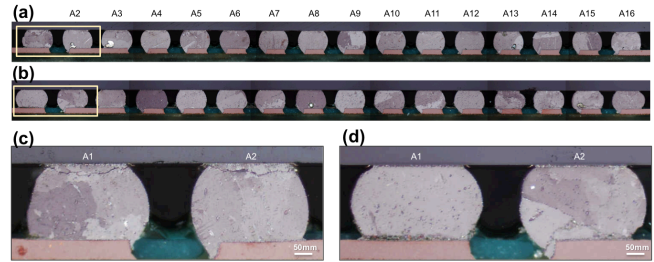

Figure 5. Edge row cross section optical polarized images after thermal cycling. (a) no-material applied component, (b) edgebond material applied component and (c)(d) higher magnification optical images from (a) and (b). [2]
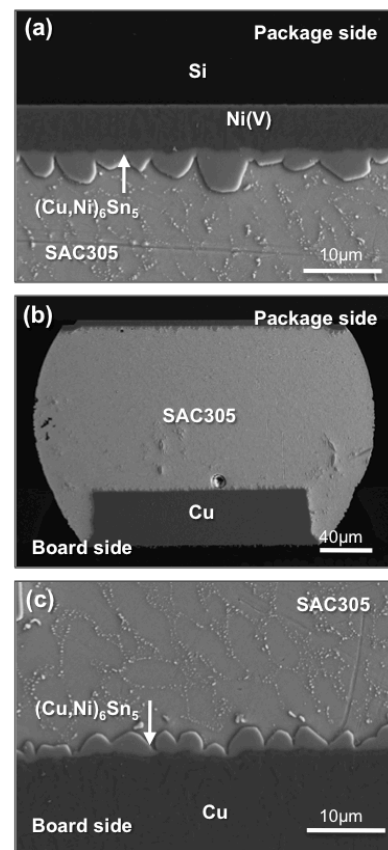

Figure 6. Initial microstructure SEM picture before thermal cycling.

localized temperature under the component to 80°C with a nominal electric current. The elevated temperature for this study was fixed to 50°C. Figure 7 shows the schematic drawings of the heater cover area and the test sample configurations. The heater covered the area of 10x10mm below the component and the test temperature of 50°C
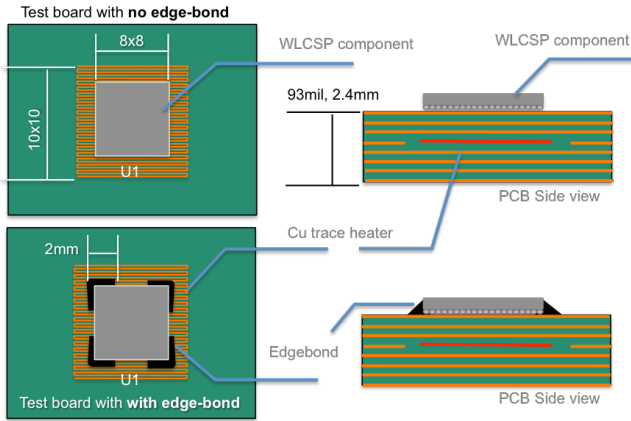
Figure 7. Schematic drawing of edgebond applied and no edgebond material applied 8x8mm WLCSP sample configuration. The Cu trace heater is located at the 4th layer of the PCB with a 10x10mm area coverage.
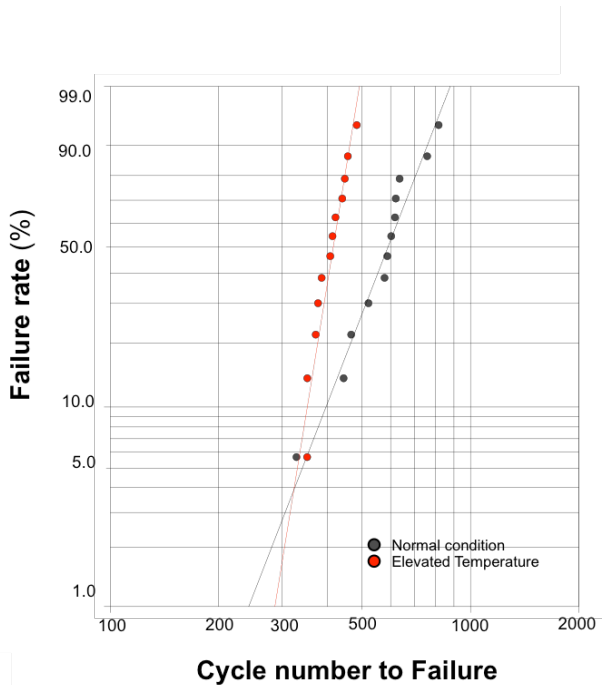

Figure 8. Weibull plot of thermal cycled 8x8mm WLCSP with normal temperature range and elevated temperature thermal cycling profile.

modified the thermal cycling temperature profile from 0 ^{o}C~100 ^{o}C to a thermal cycling profile of ~25 ^{o}C to 125°C. Figure 8 shows the Weibull plot for the normal temperature and elevated temperature thermally cycles samples. Due to the higher temperature range during thermal cycling, the lifecycle number degraded from 638 cycles characteristic cycle to 430 cycles, a 33% degradation of life cycle

numbers. But the first failure cycle numbers were similar with actually an earlier first failure cycle number for the normal temperature thermal cycling with 331 cycles. The first failure cycle for the elevated temperature thermal cycling was 355 cycles. Figure 9 shows the SEM picture of a failed solder joint for 8x8mm WLCSP tested with elevated temperature thermal cycling. The crack propagation can be seen at the package side interface with an extended Cu and IMC depletion zone near the package side. This depletion zone can be observed in isothermal aged samples [5-7] where the thermal aging induced the Cu diffusion towards the IMC interface at the package side due to lower Gibbs free energy needed, to form the $(Cu,Ni)_6Sn_5$ IMC.[8] The microstructure observed here shows the similar mechanism, which also contributed to the accelerated crack propagation at the package side interface.[9-12] To compare the overall grain recrystallization rate and the test condition, area of grain refinement and recrystallization were identified and measured as shown in Figure 10(a). An optical picture and polarized image were used to identify the recrystallization region and a mesh overlapped to the polarized image was used to locate and measure the strain induced recrystallization area. Figure 10(b) is the recrystallization region map for solder joint A1 to A4, which are the joints from a 8x8mm WLCSP sample tested at normal thermal cycling condition. A1 joint is the outmost corner joint. As shown, recrystallization regions can be seen at interface near the package side, which are indicated in orange boxes, for all four solder joints from the corner, mostly at the package side interface region. Compared to the normal condition thermal cycled sample, Figure 10(c) shows the recrystallized region distribution for the elevated temperature tested samples. A more widely distributed grain recrystallization region can be found, indicating a more active strain induced damage accumulation during thermal cycling. For both samples, the outer most corner joints were the most damage accumulation joints, which is aligned with the earlier observation in 7x7mm WLCSP samples. To mitigate and strengthening the corner joints for both cases, Edgebond B material with higher Tg, 130°C and lower CTE, 30ppm/^{o}C were applied and tested for the same thermal cycling conditions. The main purpose of applying a higher Tg and lower CTE material was to enhance the stability of the WLCSP not only at room temperature but also at elevated temperature like the case demonstrated here at 50°C. Figure 11 is the Weibull plot for indicating the failure distribution of the edgebond B material applied WLCSP samples. As shown in Figure 11, only one failure was observed for the elevated temperature thermal cycled samples, until reaching 2000 cycles and no failure were identified with normal temperature thermal cycling. With
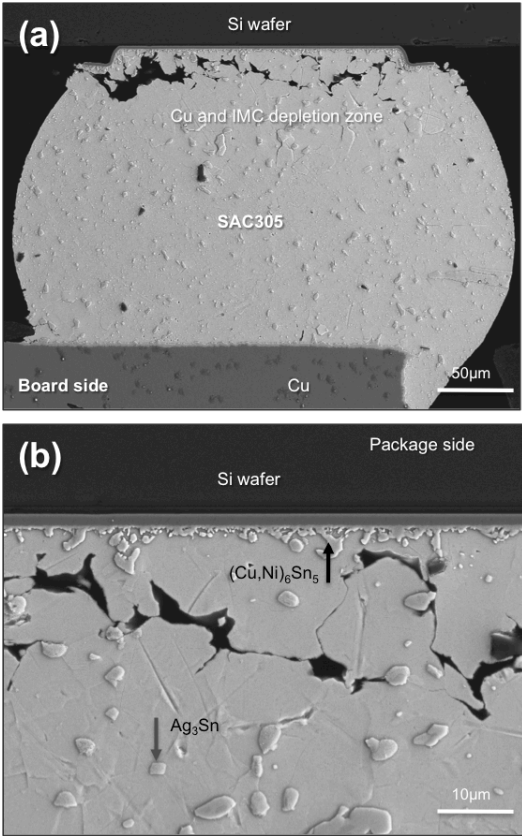
Figure 9. SEM image of failed solder joint after thermal cycling at elevated temperature. (a) overall solder joint, (b) package side interface region.

Figure 10. Recrystallized region measurement and indication for A1 to A4 joints for each thermal cycling conditions. (a) Rx region indication example, (b) Rx region for normal temperature thermal cycled sample from A1 to A4 joint. (c) for elevated temperature thermal cycled sample.

2000 cycles no failure for the normal condition thermal cycling, it is already a ~300% improvement of thermal cycling performance subject to first failure cycle number. The test is scheduled to extend for further cycles to complete the failure distribution and associated characteristic life cycle number. Further analysis to find the enhancement mechanism will be a task to pursue.
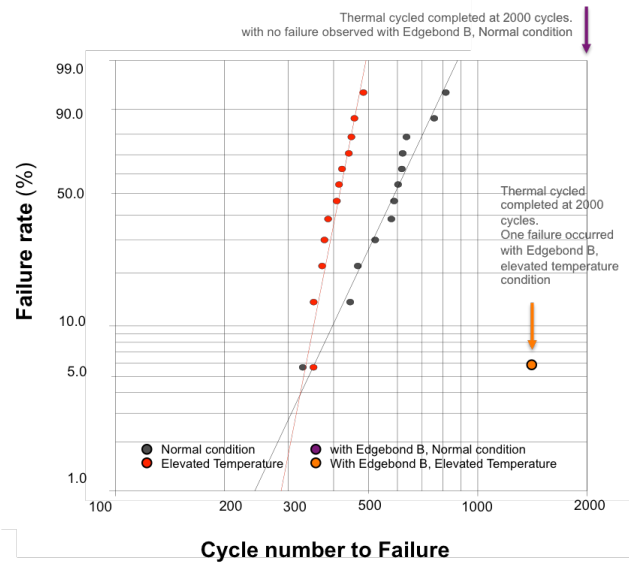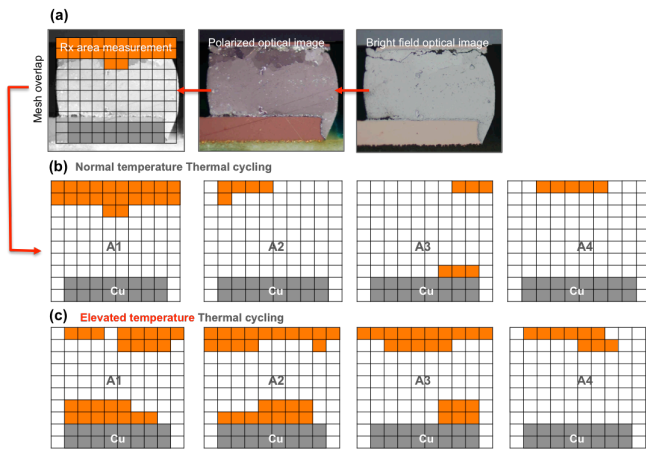

Figure 11. Weibull plot of thermal cycled 8x8mm WLCSP with Edge-bond B material applied for normal temperature range and elevated temperature thermal cycling.

IV. CONCLUSIONS

The demand on reliable Wafer level chip scale packages (WLCSP) are getting higher due to the need of small form factor and cost. The mechanism, leading to crack initiation and propagation during thermal cycling by sub-grain boundary development can be observed as a general damage accumulation mechanism in various solder joints, can be observed in the series of tested samples in this study. The correlation between crack propagation and localized recrystallization are compared in a series of cross section analyses on thermal cycled WLCSP components with normal and elevated temperature thermal cycling conditions. Damage accumulated solder joint locations are identified and an attempt of using edge-bond materials to strengthen the localized solder joints demonstrate that the higher T_g with 130°C and lower CTE with 30ppm/^{o}C is enhancing the

thermal cycling performance. It is demonstrated that Edge-bond material applied components show either a shift of damage accumulation to a more localized region, thus potentially accelerated the degradation, or mitigate the distribution resulting in an enhancement of thermal cycling based on their T_g and CTE properties. To simulate the function temperature environment, components were also tested at elevated temperature of 50^oC addition to the thermal cycling profile temperature. The elevated temperature environment shows a 33% degradation of the component lifecycle, which can be improved using high T_g and low CTE edge-bond material. The results show that the crack propagation distribution and recrystallization region correlation can explain the enhancement and potential degradation mechanisms and support the damage accumulation history in a more efficient way.

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